A First Multigigahertz Digitally Controlled Oscillator for Wireless Applications

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***Abstract*—A novel digitally controlled oscillator (DCO) architecture for multigigahertz wireless RF applications, such as short-range wireless connectivity or cellular phones, is proposed and demonstrated. It deliberately avoids any use of an analog tuning voltage control line. Fine frequency resolution is achieved through high-speed dithering, yet the resulting spurious tones are very low. This enables to employ fully digital frequency synthesizers in the most advanced deep-submicrometer digital CMOS processes, which allow almost no analog extensions. It promotes cost-effective integration with the digital back-end onto a single silicon die. The demonstrator test chip has been fabricated in a digital 0.13-μm CMOS process together with a digital signal processor to investigate noise coupling. The 2.4-GHz DCO core consumes 2.3 mA from a 1.5-V supply and has a very large tuning range of 500 MHz. The phase noise is −112 dBc/Hz at 500-kHz offset. The presented ideas have been incorporated in a commercial BLUETOOTH transceiver.**

***Index Terms*—CMOS digital integrated circuits (ICs), digital control, digitally controlled oscillator (DCO), MOS varactor, voltage-controlled oscillators (VCOs).**

I. INTRODUCTION

TRADITIONAL designs of commercial frequency synthesizers for multigigahertz mobile RF wireless applications have almost exclusively employed the use of a charge-pump phase-locked loop (PLL), which acts as a local oscillator (LO) for both a transmitter and receiver. Unfortunately, the design flow and circuits techniques required are quite analog intensive and utilize process technologies that are incompatible with a digital baseband, which, today, is built in a low-voltage deep-submicrometer digital CMOS process with almost no analog extensions and very limited voltage headroom. Furthermore, the charge-pump-based PLL suffers from reference spurs due to its specific method of correlative phase comparison [1].

The aggressive cost and power reduction of a mobile wireless solution can only be realistically achieved by the highest level of integration, and this favors digitally intensive approach. A digitally controlled oscillator (DCO) that deliberately avoids any analog tuning voltage controls is presented in this paper. This allows for its loop control circuitry, including loop filter, to be implemented in a fully digital manner.

Thus far, there have not been any reports in the literature (except recently by the authors in [2]) on the *fully* digital control of oscillators for RF applications. Lack of the fully digital control is a severe impediment for the total integration in a deep-submicrometer CMOS process. There have been several disclosures on ring-oscillator-based DCOs for clock recovery and clock generation applications [3], [4]. However, the frequency resolution is low and the spurious tone level is high for these DCOs, which seem to become an effective deterrent against digital RF synthesizers for wireless communications. The proposed combination of various circuit and architectural techniques has brought to fruition a fully digital solution that has a fine frequency resolution with low spurious content and low phase noise.

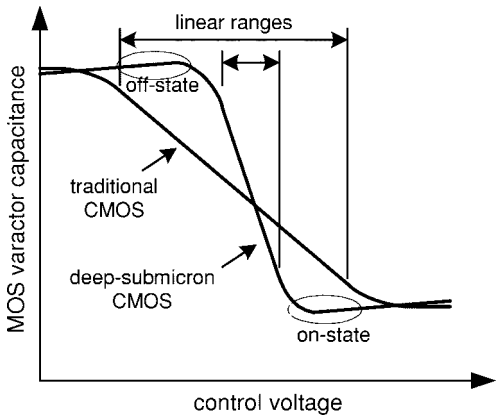

Fig. 1. Idealized capacitance versus voltage curves of a MOS varactor for both a traditional and a deep-submicrometer CMOS process.

This paper is organized as follows. Section II discusses choices behind the selected varactor and its proposed mode of operation. Section III proposes a novel fully digital manner of an *LC*-tank oscillator control. *LC*-tank details are presented in Section IV. The oscillator core is described in Section V. Section VI derives an equation for the DCO switching spurs and shows through some scenario examples that the resulting spurs could be made vanishingly small. An alternative view of the DCO oscillator as a digital-to-frequency converter is given in Section VII. The implementation and measured results are presented in SectionsVIII and IX.

II. VARACTOR IN A DEEP-SUBMICROMETER CMOS PROCESS

Frequency tuning of a low-voltage deep-submicrometer CMOS oscillator is quite a challenging task due to its highly nonlinear frequency-versus-voltage characteristics and low-voltage headroom. Fig. 1 shows normalized representative curves of a MOS varactor capacitance versus control voltage

Manuscript received April 16, 2003; revised June 15, 2003.

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Digital Object Identifier 10.1109/TMTT.2003.818579

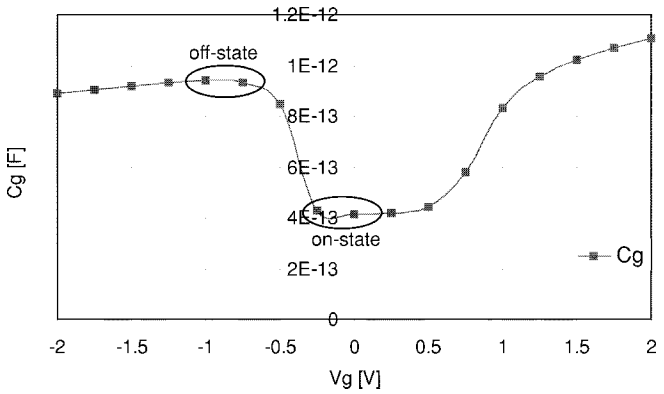

Fig. 2. Gate capacitance versus gate voltage of a measured PMOS varactor when its source, drain, and well tie-offs are tied to ground: PPOLY/NWELL, inversion type, single-contacted gate, $L = 0.5\ \mu$m, $W = 0.6\ \mu$m, $N = 8$ fingers $\times\ 12\ \times\ 2$, freq $= 2.4$ GHz.

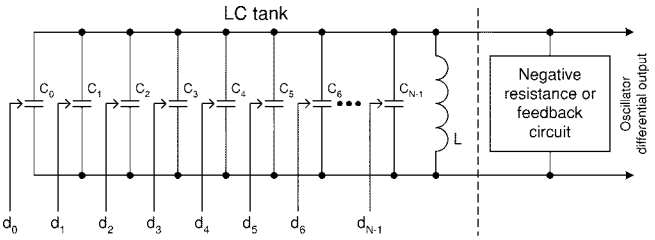

Fig. 3. *LC*-tank-based oscillator with switchable capacitors.

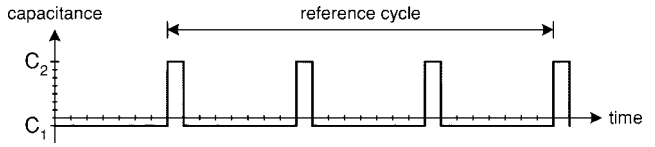

Fig. 4. DCO dithering by changing the discrete capacitance at high rate.

(*C–V*) curve for both a traditional CMOS process and a deep-submicrometer process. Previously, a large linear range of the *C–V* curve could be exploited for a precise and wide operational control of frequency. With a deep-submicrometer process, the linear range is now very compressed and has undesirable high gain ($K_{\rm VCO} = \Delta f/\Delta V$), which makes the oscillator extremely susceptible to noise and operating point shifts.

An example *C–V* curve of an actual PMOS varactor used in the proposed design for the acquisition mode is shown in Fig. 2. Due to the well isolation properties in this N-well process, the PMOS device is a better candidate for a varactor. It was experimentally confirmed that, in this process, the PPOLY/NWELL inversion-type varactor features more distinctly defined operational regions than does the accumulation-type varactor. In fact, the flat on-state region of the depletion mode and the flat off-state region of the inversion mode (Fig. 2) are used as two stable binary-controlled operating points. Advanced CMOS process lithography today allows the creation of extremely small-size, but well-controlled varactors. The switchable capacitance of the finest differential least significant bit (LSB) varactor is on the order of tens of attofarads. The slight drop of capacitance in the "flat" strong inversion region had not been of any practical significance until the advent of deep-submicrometer CMOS processes. It is due to the depletion layer being created in the gate polysilicon [5], which is less doped and much thinner than in the past.

III. Fully Digital Control of Oscillating Frequency

The proposed solution [2] to control the oscillating frequency could generally be summarized as follows. A method of weighted binary switchable capacitance devices, such as varactors, is proposed. An array of varactors (Fig. 3) could be switched into a high-capacitance mode or a low-capacitance mode individually by a two-level digital control voltage bus, thus giving a very coarse step control for the more-significant bits, and less coarse step control for the less-significant bits. In order to achieve a very fine frequency resolution, the LSB bit could possibly be operated in an analog fashion, as demonstrated in [6]. However, this requires a fine-resolution digital-to-analog converter (DAC) or a charge-pump PLL with voltage-controlled oscillator (VCO) gain ($K_{\rm VCO}$) linearization circuits. A better solution is to dither the LSB digital control bit (or multiple bits), thus controlling its time-averaged value to achieve a finer resolution. Consequently, each varactor could be allowed to stay in only one of the two regions where the capacitance sensitivity is the lowest and the capacitance difference between them is the highest. These two operating regions are shown by the ovals in Fig. 2.

The proposed idea of high-rate dithering of LSB capacitors is illustrated in Fig. 4. Instead of applying a constant input that would select capacitance C_1 or C_2, where $C_2 = C_1 + \Delta C$ with ΔC being an LSB capacitor, during the entire reference cycle, the selection alternates between C_1 and C_2 several times during the cycle. In the example, C_2 is chosen one-eighth of the time and C_1 is chosen the remaining seven-eighths. The average capacitance value, therefore, will be one-eighth of the $C_2 - C_1$ distance over C_1. It should also be noted that the resolution of the time-averaged value relies on the dithering speed. Without any feedback that would result in a supercycle, the dithering rate has to be higher than the reference cycle rate times the integer value of the resolution inverse (eight in this case). Therefore, there is a proportional relationship between the frequency resolution improvement and the dithering rate.

The dithering pattern shown in Fig. 4 is not random at all and is likely to create spurious tones. It is equivalent to the first-order $\Sigma\Delta$ modulation [7]. Section VI addresses the DCO varactor switching spurs. A second and third order of $\Sigma\Delta$ randomization is used in order to effectively eliminate the already low spurious content.

IV. *LC* Tank

The idea of the digitally controlled *LC* tank oscillator is shown from a higher system level in Fig. 3. The resonating frequency of the parallel *LC* tank is established by the following formula:

$$f = \frac{1}{2\pi\sqrt{L \cdot C}}. \tag{1}$$

The oscillation is perpetuated by a negative resistance device, which is normally built as a positive feedback active amplifier network.

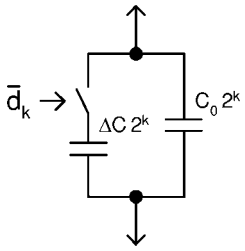

Fig. 5. Binary-weighted switchable capacitor of index k.

The frequency f could be controlled by either changing the inductance L or the capacitance C. However, in a monolithic implementation, it is more practical to keep the inductor fixed while changing capacitance of a voltage-controlled device, such as a varactor. Since the digital control of the capacitance C is required, the total capacitance is quantized into an N number of smaller digitally controlled varactors, which do not necessarily follow the binary-weighted pattern of their capacitance values. Equation (1) now becomes

$$f = \frac{1}{2\pi\sqrt{L \cdot \sum_{k=0}^{N-1} C_k}}. \tag{2}$$

The digital control signifies that each of the individual capacitors (of index k) could be placed in either a high capacitative state $C_{1,k}$ or a low capacitative state $C_{0,k}$ (see Fig. 1). The capacitance difference between the high and low capacitative states of a single-bit k is $\Delta C_k = C_{1,k} - C_{0,k}$ and is considered the effective switchable capacitance. Since the frequency of oscillation grows with lowering the capacitance, increasing the digital control value must result in the increased frequency of oscillation. Therefore, the digital control state is opposite to the capacitative state so the digital bits need to be *inverted* such that the kth capacitor could be expressed as

$$C_k = C_{0,k} + \overline{d_k} \cdot \Delta C_k.$$

The bit inversion turns out to be quite convenient from the implementational point-of-view. It will be later shown in Section V that it is necessary to provide a buffering scheme that would: 1) isolate the "raw" varactor input from the noisy digital circuits; 2) have sufficiently low driving resistance to minimize the thermal and flicker noise; and 3) establish two stable low- and high-voltage levels for the best varactor operation. Equation (2) could be rewritten to include the digital control details as follows:

$$f = \frac{1}{2\pi\sqrt{L \cdot \sum_{k=0}^{N-1} \left(C_{0,k} + \overline{d_k} \cdot \Delta C_k\right)}}. \tag{3}$$

Fig. 5 shows a model of a single-cell binary-weighted switchable capacitor of index k that is equivalent to the weight of 2^k. The basic unit cell is created for the weight of 2^0. The next varactor of weight 2^1 is created not as a single device of double the unit area, but it is built of two unit cells. This is done for matching purposes. It mainly ensures that the parasitic capacitance due to fringing electric fields, which is quite significant for a deep-submicrometer CMOS process and is extremely difficult to control and model, is well ratioed and matched. Each next cell consists of double the number of the unit cells. Even though the total occupied silicon area of the device multiplicity method is somewhat larger than the straightforward method of progressively larger uniform devices, it allows to easily achieve the economical component matching resolution of 8 bits.

When the d_k digital control bit is one, the only capacitance seen by the oscillating circuit is C_0 times the weight. This capacitance is always present signifying that the varactor could never be truly turned off. For this reason it could be considered a "parasitic" shunt capacitance. The total sum of these contributions $C_{0,\mathrm{tot}}$ sets the upper limit of the oscillating frequency for a given inductance L. When the digital control bit is zero, the ΔC capacitance times the weight is added. The index k of the binary-weighted capacitance can thus be described as

$$C_k = C_{0,k} \cdot 2^k + \overline{d_k} \cdot \Delta C_k \cdot 2^k \tag{4}$$

making the total binary-weighted capacitance of size N

$$\begin{aligned} C &= \sum_{k=0}^{N-1} C_k \\ &= \sum_{k=0}^{N-1} \left(C_{0,k} \cdot 2^k + \overline{d_k} \cdot \Delta C_k \cdot 2^k\right) && (5) \\ &= \sum_{k=0}^{N-1} C_{0,k} \cdot 2^k + \sum_{k=0}^{N-1} \overline{d_k} \cdot \Delta C_k \cdot 2^k && (6) \\ &= C_{0,\mathrm{tot}} + \sum_{k=0}^{N-1} \overline{d_k} \cdot \Delta C_k \cdot 2^k. && (7) \end{aligned}$$

Contributions from all the static shunt capacitances are lumped into $C_{0,\mathrm{tot}}$ so the only adjustable components are the effective capacitances in the second term of (7).

V. Oscillator Core

For the process technology being used to fabricate the proposed DCO, $1/f$ noise does not have a consistent trend both across all allowed voltage ranges (V_{DS} and V_{GS}) defined by the process, and between NMOS and PMOS transistors. That is: 1) the K_f factor has a bias dependence and 2) compared to a PMOS transistor, an NMOS transistor could have a lower $1/f$ noise at one bias condition while having a higher $1/f$ noise at another bias condition. With the concerns of $1/f$ noise being high in a deep-submicrometer CMOS process and the PLL bandwidth being typically lower than the $1/f^3 - 1/f^2$ corner of an oscillator spectrum skirt for modern wireless applications, the DCO was implemented to operate in a voltage swing range having a lower $1/f$ noise. Since an oscillator naturally operates with a large voltage swing and the transistors experience linear, saturation, and cutoff bias conditions, a complementary cross-coupled structure was used [see Fig. 6(a)] to average the $1/f$ noise contribution between NMOS and PMOS transistors at different bias conditions. The complementary structure also has an advantage of producing more g_m with the same amount of current, thus reducing the overall power consumption. On the other hand, the transistors were sized such that each of the

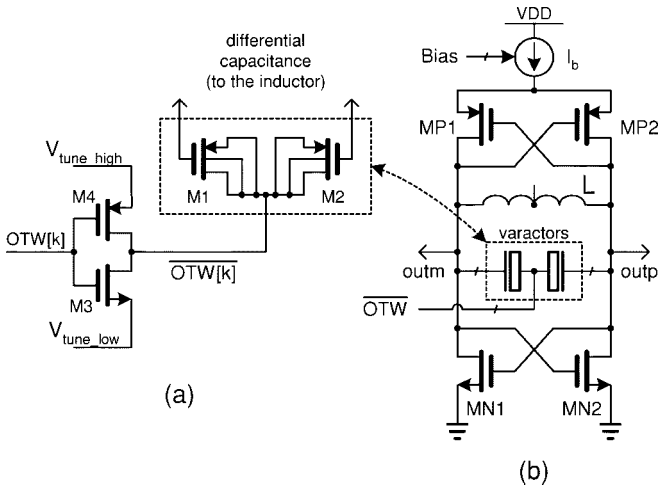

Fig. 6. (a) Differential varactor and an inverting driver. (b) Ideal schematic of the DCO oscillator core.

NMOS and PMOS pairs generates about one-half of the total g_m. Consequently, the overall thermal noise is lower than that using only an NMOS pair to produce g_m [8].

Cross-coupled transistors MP1-2 and MN1-2 form a positive feedback loop to provide negative resistances to cancel the *LC*-tank loss sustaining the oscillation. The oscillator core current source is implemented with binary-weighted transistors controlled by digital bits with an automatic calibration algorithm to set the optimal operating condition. Generally, the greater the oscillator core bias current I_b, the better phase noise performance. However, with the particular topology used for this DCO, once the I_b bias current exceeds a certain threshold where the oscillator voltage swing approaches V_{DD} and V_{SS} supply levels, it will start causing waveform distortion, thus leading to degradation in the phase noise and spurious levels. On the low side of I_b, a minimum setting should be observed to merely ensure the oscillation. This serves as a basis for the automatic calibration algorithm. The I_b bias current is digitally swept to find the oscillation cutoff mark. A certain predetermined offset is then added to the binary control value. The offset value was experimentally obtained based on statistics of a large number of devices to guarantee a satisfactory phase noise performance level. This method is considered a simpler alternative to setting the bias algorithmically while directly searching for an acceptable phase noise performance at the lowest amount of bias current. It should be noted that the oscillator exceeds the phase noise performance requirements of the targeted BLUETOOTH standard by a large margin for a very wide range of devices and the bias current settings so the above algorithm is meant to simultaneously improve production yield and current consumption.

As will be described below, a clock squarer is used to convert the sinusoidal oscillator waveform to a square wave to further drive digital logic and output buffers for measuring the DCO performance. To suppress the thermal noise of the current source at $n\omega_0$, where $n > 0$, as well as the noise coming from V_{DD} and $V_{\rm tune}$ lines, which could contribute to both phase noise and spurs (if the noise has specific frequency contents), decoupling capacitors are attached to the source node of the PMOS transistors, as well as the V_{DD} and $V_{\rm tune}$ lines. The *LC* tank is formed by a metal 3–5 octagonal structure inductor, a 2-pF varactor, and the parasitic capacitance of the inductor and transistors. Since a regular spiral inductor has a significant difference between y_{11} and y_{22}, the inductor layout was done in a symmetric fashion between ports 1 and 2 (center-tap inductor) to reduce the mismatch between $\rm outp$ and $\rm outm$ [9]. The measured inductor Q is approximately six at 2.4 GHz.

Fig. 6(a) shows an implementation of the differential varactor and the preceding driver stage. The $V_{\rm tune\_high}$ and $V_{\rm tune\_low}$ rail supply levels of the inverter are set to correspond with the two stable operating points, off and on states of the oscillator tuning word (OTW), respectively, as shown in Fig. 2. The varactor used in this study is a differential configuration built upon the basic structure described in conjunction with Figs. 1 and 2. The balanced capacitance is between the gates of both PMOS transistors $M1$ and $M2$ [see Fig. 6(a)], whose source, drain, and backgate connections are shorted together and tied to the $M3/M4$ inverter output. Since the voltage control is now applied to the backgate and source/drain, the negative and decreasing values of V_g in Fig. 2 ($= V_{\rm gs}$, since the source is grounded) covering the inversion mode are of interest. Due to the differential configuration, only one-half of the single PMOS capacitance is achieved, which actually enhances frequency resolution.

Since the supply voltage is only 1.5 V, as described in Section II, the varactor *C–V* curve is desired to be as steep as possible. Since the DCO voltage swing is limited to approximately 1 V_{pp}, the voltage span between maximum and minimum frequencies, if operating the DCO as a VCO by biasing $\overline{\rm OTW}$ with a variable voltage source, is only slightly larger than that of the varactor *C–V* curve. The varactor can easily be biased at the two $K_{\rm VCO} = \Delta f/\Delta V = 0$ points on a frequency versus control voltage curve with the 1.5-V power supply. The measured frequency pushing is approximately 600 kHz/V, which is low, resulting in a low sensitivity to power supply $V_{\rm tune\_low}$ and $V_{\rm tune\_high}$ noise. Therefore, the overall spurious tones and phase noise can be reduced, and the steep *C–V* curve, as well as the large $K_{\rm DCO} = \Delta f$/bit, is not a concern at all. With a dc level of approximately 0.5 V at $\rm outp$ and $\rm outm$, it was found that the optimal $V_{\rm tune\_low}$ is approximately 0.45 V and the optimal $V_{\rm tune\_high}$ is very close to, but not quite equal to, 1.5 V. Hence, in this experiment, $V_{\rm tune\_high}$ was tied to V_{DD} for simplicity and the frequency pushing from $V_{\rm tune\_high}$ is higher than $V_{\rm tune\_low}$. The varactor was also implemented in a differential fashion such that the ac current carrying the oscillation frequency only flows through the shared silicide/diffusion instead of through diffusion, silicide, contact, and metal layers between the two capacitor bottom plates [see Fig. 6(a)] resulting in a better Q. With a targeted phase noise of -110 dBc/Hz at 500-kHz offset from a 2.4-GHz carrier and with a targeted frequency tuning range of greater than 20%, it was determined that the varactor Q only needs to be >17. The dimension of each varactor gate finger was designed using the formula in [10] with an additional consideration of interconnect resistance. The actual measured frequency tuning range is 23% and the phase noise is -112 dBc/Hz at the targeted condition, as will be shown below. With the differential varactor design, the phase noise contribution due to the varactor driver $M3$ and $M4$ is small. The only concern is that the driver needs to be large enough to handle the current spike

when switching a large bank of varactors. However, since the update rate for a big varactor bank is not very high and only happens at acquisition, the driver layout size is still smaller than the varactor itself. The significant, but reasonable driver size also lowers its own noise contributing to the overall phase noise.

VI. Spurs Due to DCO Switching

Let us assume a sinusoidal modulating signal

$$g(t) = g_{\rm pk}\cos w_m t. \tag{8}$$

For a frequency modulation (FM), the instantaneous frequency ω_i is the carrier frequency ω_c modified by the modulating signal times the FM constant k_f as follows:

$$\omega_i(t) = \omega_c + k_f g(t) = \omega_c + g_{\rm pk}k_f\cos w_m t. \tag{9}$$

Defining a new constant called the peak frequency deviation

$$\Delta\omega_{\rm pk} = g_{\rm pk}k_f \tag{10}$$

we can rewrite (9) as

$$\omega_i(t) = \omega_c + \Delta\omega_{\rm pk}\cos w_m t. \tag{11}$$

The phase of this FM signal is

$$\theta(t) = \omega_c t + \frac{\Delta\omega_{\rm pk}}{\omega_m}\sin w_m t = \omega_c t + \beta\sin\omega_m t \tag{12}$$

where

$$\beta = \frac{\Delta\omega_{\rm pk}}{\omega_m} \tag{13}$$

is a dimensionless ratio of the peak frequency deviation to the modulating frequency. The resulting signal is

$$s_{\rm FM}(t) = A\cos(\omega_c t + \beta\sin\omega_m t). \tag{14}$$

Equation (14) could be rewritten after some trigonometric expansion as follows:

$$s_{\rm FM}(t) = A\cos(\omega_c t)\cos(\beta\sin\omega_m t) - A\sin(\omega_c t)\sin(\beta\sin\omega_m t). \tag{15}$$

For small values of β (narrow-band frequency modulation (NBFM) modulation), we can make the following approximations:

$$\cos(\beta\sin\omega_m t) \approx 1 \tag{16}$$

$$\sin(\beta\sin\omega_m t) \approx \beta\sin\omega_m t. \tag{17}$$

Substituting these into (15), we obtain an approximate solution for small β

$$s_{\rm NBFM}(t) = A\cos(\omega_c t) - \beta A\sin(\omega_m t)\sin(\omega_c t). \tag{18}$$

Expanding (18) into phasor form, we have

$$s_{\rm NBFM}(t) = \Re\left\{Ae^{j(\omega_c t)}(1 + j\beta\sin\omega_m t\right\} = \Re\left\{Ae^{j(\omega_c t)}\left(1 + \frac{1}{2}\beta e^{j\omega_m t} - \frac{1}{2}\beta e^{-j\omega_m t}\right)\right\}. \tag{19}$$

From (19), it is clearly seen that the power spectral density of an NBFM signal is the continuous-wave carrier frequency plus two sidebands ω_m away and $20\log((1/2)\beta)$ dB below the carrier.

Let us apply the above analysis of an NBFM to our specific case of dithering the oscillating frequency of an *LC* tank by switching a unit capacitor value through a digital control (see Fig. 5). When the control signal is high, the capacitor value is $C_{\rm on}$ and the oscillating frequency is

$$f_{{\rm osc},h} = \frac{1}{2\pi\sqrt{LC_{\rm on}}}. \tag{20}$$

Similarly, when the control signal is low, the capacitor value is $C_{\rm off}$ and the oscillating frequency is

$$f_{{\rm osc},l} = \frac{1}{2\pi\sqrt{LC_{\rm off}}}. \tag{21}$$

The difference between the high and low oscillation frequencies is

$$\Delta f_{pp} = f_{{\rm osc},h} - f_{{\rm osc},l}. \tag{22}$$

The peak angular frequency deviation is

$$\Delta\omega_{\rm pk} = 2\pi\frac{\Delta f_{pp}}{2}. \tag{23}$$

The modulating signal frequency is ω_m.

The NBFM analysis assumed thus far a sinusoidal modulating signal $g(t)$ in (8). However, the FM function of turning on and off a small unit-size capacitor is obviously a rectangular wave ($g_{\rm rect}(t)$ assumed of unity peak-to-peak amplitude)

$$\Delta\omega(t) = \Delta\omega_{pp}\cdot g_{\rm rect}(t) \tag{24}$$

with the following zero-mean trigonometric Fourier series decomposition

$$g_{\rm rect}(t) = \sum_{n=1}^{\infty} a_n\cos n\omega_m t \tag{25}$$

where

$$a_n = 2\cdot\frac{\tau}{T}\cdot{\rm sinc}\left(\frac{n\pi\tau}{T}\right) \tag{26}$$

is the nth coefficient of the trigonometric Fourier series representation, and ${\rm sinc}(x) \equiv \sin(x)/x$. $T = 2\pi/\omega_m$ and τ are the period and the turn-on time, respectively, of the rectangular wave. For a special case of the symmetric square wave, $\tau = 1/2$ and (25) becomes

$$g_{\rm square}(t) = \sum_{n=1,{\rm odd}}^{\infty}\frac{2}{\pi}\frac{1}{n}\cdot\sin n\omega_m t. \tag{27}$$

The modulation index of the nth harmonic is now adjusted for the Fourier series decomposition of a rectangular switching wave

$$\beta_n = \frac{a_n}{n}\frac{\Delta\omega_{pp}}{\omega_m}. \tag{28}$$

In most cases, especially with a balanced duty cycle, only the fundamental component would really matter. It should be noted that the frequency modulating wave $g_{\rm rect}(t)$ in a deep-submicrometer CMOS process at 2.4 GHz is actually a trapezoidal waveform, but with very sharp edge transitions.

1) Example I: Let us consider an example of switching the oscillating frequency by $\Delta f_{pp} = 23$ kHz at the clock rate of 600 MHz. Let us consider the first harmonic in the Fourier series decomposition whose peak amplitude is $2/\pi$ times the square wave peak-to-peak amplitude. The modulating frequency is one-half of the clock direction switching rate, i.e., $f_m = \omega_m/2\pi = 300$ MHz,

$$\beta_1 = a_1 \frac{\Delta f_{pp}}{f_m} = \frac{2}{\pi} \cdot \frac{23\text{ kHz}}{\frac{600\text{ MHz}}{2}} = 4.88 \cdot 10^{-5}. \quad (29)$$

This gives rise to spurs 300 MHz away on both sides from the oscillating frequency. Their power level is at

$$20 \log\left(\frac{\beta_1}{2}\right) = -92.3\text{ dB}$$

relative to the carrier. This scenario reflects the actual implementation.

The above -92.2-dBc spur level corresponds to the situation when the DCO is dithered continuously at the highest possible rate. Obviously, this is not a practical case. In fact, the $\Sigma\Delta$ dithering will randomize the spurious energy and blur it into the background.

2) Example II: Let us consider now the case of performing the same switching, but at the 13 MHz of a commonly used frequency reference (FREF)

$$\beta_1 = \frac{2}{\pi} \cdot \frac{23\text{ kHz}}{\frac{13\text{ MHz}}{2}} = 2.25 \cdot 10^{-3}$$

and the spur power level is much higher now at

$$20 \log\left(\frac{\beta}{2}\right) = -59.0\text{ dB}.$$

VII. Open-Loop Narrow-Band Digital-to-Frequency Conversion (DFC)

From the functional perspective, the above operation can be thought of as a DFC with the digital word comprising d_k bits, where $k = 0, 1, \ldots, N-1$, directly controlling the output frequency f. In order to illustrate that a straightforward linear DFC conversion to the RF range is not likely to work, let us consider the following example. For the BLUETOOTH application with the oscillating frequency in the RF band of 2.4 GHz and a frequency resolution of 1 kHz, at least 22 bits of DFC resolution is required. It is clearly utmost difficult to achieve this kind of precision even with the most advanced component-matching techniques. The best one could hope to economically achieve is 8–9 bits of capacitor matching precision [11], without resorting to elaborate matching schemes that often require numerous and time-consuming design, layout, and fabrication cycles. In fact, better than 10-bit resolution would normally require some digital error correction techniques [12].

There is one aspect of DFC for wireless communications that significantly differs from the general digital-to-analog conversion and that is taken advantage of here. Namely, it is the narrow-band nature of the wireless communication transmission. Consequently, even though the frequency command steps must be very fine, the overall dynamic range at a given time instant is quite small. For example, the nominal frequency deviation of the BLUETOOTH Gaussian frequency shift-keying (GFSK) data modulation scheme is 320 kHz. For a 1-kHz frequency resolution, only 9 bits could be made required ($320\text{ kHz}/1\text{ kHz} = 320 < 2^9$). If not handled carefully, a much higher dynamic range is usually necessary to cover frequency channels of the RF band. For the BLUETOOTH band of 80 MHz, 17 bits of full 1-kHz resolution are thus required. Many more extra bits would be necessary to account for process and environmental (voltage and temperature) changes that could reach over $+/-20\%$ of the operational RF frequency.

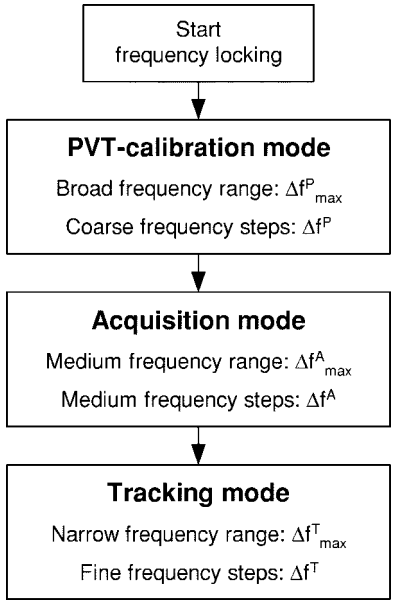

Fig. 7. Progression flowchart of the DCO operational modes.

The proposed solution to the above dynamic-range problem is to proportionately lower the frequency resolution whenever a higher dynamic range is expected. This is accomplished by traversing through the three major operational modes with progressively lower frequency range and higher resolution such that the intrinsically economical component matching precision of 8 bits is maintained (Fig. 7). In the first step, the large oscillating frequency uncertainty due to the process-voltage-temperature (PVT) variations is calibrated. After the PVT calibration, the nominal center frequency of the oscillator will be close to the center of the BLUETOOTH band. Since this uncertainty could easily be in the hundreds of megahertz range, a 1- or 2-MHz increments are satisfactory. In this case, an 8-bit resolution is sufficient. The second step is to acquire the requested operational channel within the available band. For an 8-bit resolution, half-megahertz steps would span over 100 MHz, which is enough for the 80-MHz BLUETOOTH band.

The third step is the finest, but with the most narrow-band range, and serves to track the frequency reference and to perform data modulation within the channel. In the proposed solution, the 1-MHz channel spacing resolution of the BLUETOOTH band already starts at the first step (PVT), but because of the very coarse frequency selection grid possibly covering multiple channels, the best that could be achieved is to get near the neighborhood of the desired channel. It is in the second step (the

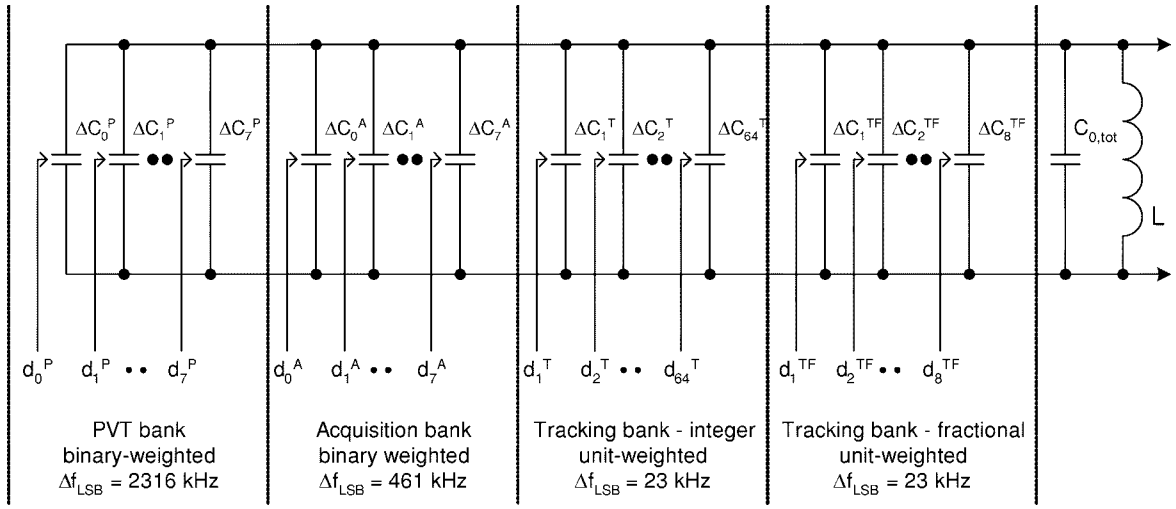

Fig. 8. *LC* tank with dedicated discrete capacitor banks for each of the three operational modes.

acquisition mode) that the channel is approximately acquired. However, the fine selection of the requested channel could only be accomplished in the third step (the tracking mode), which is most refined of them all. Therefore, the tracking mode dynamic range has to additionally cover the resolution grid of the preceding acquisition mode. For the BLUETOOTH example, if frequency in the acquisition mode cannot be resolved to better than 500 kHz and the FM range is 320 kHz, then the dynamic range of the tracking mode should be better than 10 bits $[(500\text{ kHz} + 160\text{ kHz})/1\text{ kHz} = 660 < 2^{10}]$.

From the operational perspective, the varactor array is divided into three major groups (varactor banks) that reflect three general operational modes, i.e., PVT, acquisition, and tracking. The first and second groups approximately set the desired center frequency of oscillation initially, while the third group precisely controls the oscillating frequency during the actual operation. During PVT and acquisition, the frequency range is quite high, but the required precision is relatively low; therefore, the best capacitor array arrangement here is the binary-weighted structure with a total capacitance of [based on (7)]

$$C^P = C_0^P + \sum_{k=0}^{N^P-1} \overline{d}_k^P \cdot \left(\Delta C^P \cdot 2^k\right) \tag{30}$$

$$C^A = C_0^A + \sum_{k=0}^{N^A-1} \overline{d}_k^A \cdot \left(\Delta C^A \cdot 2^k\right) \tag{31}$$

where N^P is the number of PVT-mode varactors, N^A is the number of acquisition-mode varactors, ΔC^P and ΔC^A are the unit capacitance of the LSB varactors, and $\overline{d}_k^P$ and $\overline{d}_k^A$ are the inverted PVT and acquisition bits, respectively, of the DCO tuning word that control capacitance of the varactor devices.

It is important to note that, at any given time, only varactors that belong to the same bank are allowed to switch. Consequently, only the varactors in each bank need to be matched. This is the key principle behind achieving an extremely fine digital frequency resolution with only 8-bit basic resolution of component matching.

The process/environmental subgroup corrects the center oscillating frequency of the operational band due to PVT variations and could be performed at manufacturing, on power-up or on "as-needed" basis. The channel select varactor group controls the frequency acquisition process for the desired transmission channel. Both groups are best implemented using individual binary-weighted capacitance structures, but their ranges could be overlapping. There is no need to preserve the binary-weight continuity between the process/environmental and channel select structures due to the different origin of their respective control inputs. The PVT correction is infrequent and could be usually done through register interface (e.g., lookup table created during factory calibration), whereas the channel select DCO tuning is performed dynamically and is an integral part of the synthesizer PLL loop. Fig. 8 shows the dedicated capacitor banks, which are connected in parallel to create a larger quantized capacitance. Only the effective switchable capacitors are shown forming the banks. The individual shunt capacitances are indistinguishable from each other, therefore, they are lumped together as $C_{0,\text{tot}}$. Also shown in this figure is the fractional-resolution tracking varactor bank for the high-speed dithering.

The tracking-mode operation presents, on the other hand, a different set of requirements. The frequency range is relatively low, but the required resolution is quite high. The binary-weighted capacitance arrangement of the acquisition mode is a poor choice here due to: 1) binary switching noise (changing a value by one LSB might require many bits to toggle; e.g., incrementing decimal 31 causes 6 bits to flip) and 2) poor device matching of different size devices (2× precision-matched capacitor is rarely implemented as twice the area—usually two identical devices are in parallel next to each other), etc. A better structure would be an array of unit devices of fine, but identical dimensions. The total capacitance is

$$C^T = C_0^T + \sum_{k=1}^{N^T} \overline{d}_k^T \cdot \Delta C^T \tag{32}$$

where N^T is the number of tracking-mode varactors, ΔC^T is the unit switchable capacitance of each varactor, and $\overline{d}_k^T$ are the inverted tracking bits of the DCO tuning word.

Since the relative capacitance contribution of the tracking bank is quite small as compared to the acquisition bank, the frequency deviation due to the tracking capacitors could be linearized by the df/dC derivative of (2). Consequently, the frequency resolution or granularity of the *LC* tank oscillator is a function of the operating frequency f

$$\Delta f^T(f) = f \cdot \frac{\Delta C^T}{2C} \tag{33}$$

where ΔC^T is the tracking-bank unit switchable capacitance and C is the total capacitance. The total tracking-bank frequency deviation is

$$f^T(f) = \Delta f^T \cdot \sum_{k=1}^{N^T} d_k^T = f\frac{\Delta C^T}{2C} \cdot \sum_{k=1}^{N^T} d_k^T. \tag{34}$$

The tracking-bank encoding is classified as a redundant arithmetic system since there are many ways to represent a number. The simplest encoding would be a thermometer scheme with a predetermined bit order. A less restrictive numbering scheme was chosen in order to facilitate a dynamic element matching—a technique to linearize the frequency-versus-code transfer function.

The DCO operational-mode progression could be mathematically described in the following way. Upon power-up or reset, the DCO is set at a center or "natural" resonant frequency f_c by appropriately presetting the d_k inputs. This corresponds to a state in which half or approximately half of the varactors are turned on, in order to maximally extend the operational range in both directions. The total capacitance value of the *LC* tank is C_c and the "natural" frequency is

$$f_c = \frac{1}{2\pi\sqrt{L \cdot C_c}}. \tag{35}$$

During the PVT mode, the DCO will approach the desired frequency f by appropriately setting the d^P control bits so that the new total capacitance is $C_{\mathrm{tot},P} = C_c + \Delta C^P$. The resulting final frequency of the PVT mode is

$$f_c^P = \frac{1}{2\pi\sqrt{L \cdot C_{\mathrm{tot},P}}}. \tag{36}$$

The acquisition mode will start from a new center frequency of f_c^P. It will approach the desired frequency f by appropriately setting the d^A control bits so that the new total capacitance is $C_{\mathrm{tot},A} = C_c + \Delta C^P + \Delta C^A$. The resulting final frequency of the acquisition mode is

$$f_c^A = \frac{1}{2\pi\sqrt{L \cdot C_{\mathrm{tot},A}}}. \tag{37}$$

The following tracking mode will commence from a new center frequency of f_c^A. It will reach and maintain the desired frequency f by appropriately setting the d^T control bits so that the new total capacitance is $C_{\mathrm{tot},T} = C_{0,\mathrm{tot}} + \Delta C^P + \Delta C^A + \Delta C^T$. The resulting frequency of the tracking mode is set by (1).

The above-described mode progression process of Fig. 7 contains two mode switching events during which the center frequency is "instantaneously" shifted closer and closer toward the desired frequency. At the end of the PVT and acquisition modes, the terminating-mode capacitor state is frozen and it now constitutes a new center frequency (f_c^P or f_c^A) from which the frequency offsets, during the following mode, are calculated.

The following list summarizes the three operational modes of the DCO together with their arithmetic word encoding, nominal frequency resolution, and range, as implemented in the presented integrated-circuit (IC) chip.

- *PVT-calibration mode*: Active during cold power-up and on as-needed basis. Places the nominal center frequency of the DCO in the middle of the BLUETOOTH band. It is also possible to use this mode on a regular basis as an ultrafast acquisition before the regular acquisition mode. Uses an 8-bit binary-weighted encoding. For best matching, the binary weight is obtained by means of finger multiplicity of a unit-size varactor. Frequency resolution $\Delta f^P = 2316$ kHz.
- *Acquisition mode*: Active during channel select. Uses an 8-bit binary-weighted encoding. For best matching, the binary weight is obtained by means of finger multiplicity of a unit-size varactor. Frequency resolution $\Delta f^A = 461$ kHz. Frequency range $\Delta f_{\max}^A = 118$ MHz.
- *Tracking mode*: Active during the actual transmit and receive. 64-bit unit-weighted encoding and 8-bit unit-weighted encoding for the fractional resolution. Frequency resolution $\Delta f^T = 23$ kHz corresponding to capacitative resolution of $\Delta C^T = 38$ aF, as governed by (33). Frequency range $\Delta f_{\max}^T = 1.472$ MHz.

Fig. 9 demonstrates a numerical example of the frequency transversal for the implemented DCO. Let us assume that the PVT mode has been calibrated to the middle of the BLUETOOTH band by fixing the selection to the code of 111. The acquisition mode, therefore, starts from the midpoint reset value of 128, where roughly half of the varactors are turned on and the other half are turned off. Let us further assume that the desired center frequency lies two channels or 2 MHz lower from the center channel of the BLUETOOTH band. This translates to between 4–5 acquisition steps. As a result, the loop will first quickly move several steps lower from the starting code of 128. After reaching the point about 2 MHz away, it will dither between the codes of 123 and 124, not being able to resolve any finer. In this example, the transition to the tracking mode happens when the acquisition code is 123. This code stays frozen for the duration of the packet. The tracking mode always starts from the midpoint value of 31. It happens that the desired center frequency is located about 230 kHz higher from that point. This corresponds to ten tracking steps. During transmission, another 160 kHz is allocated on both sides to the FM.

VIII. IMPLEMENTATION

The oscillator is built as an ASIC cell (Fig. 10) with truly digital I/Os, even at the RF frequency of 2.4 GHz, which has rise and fall times specified to be 50 ps. The RF signal digitizer is a differential-to-digital converter (with complementary outputs)

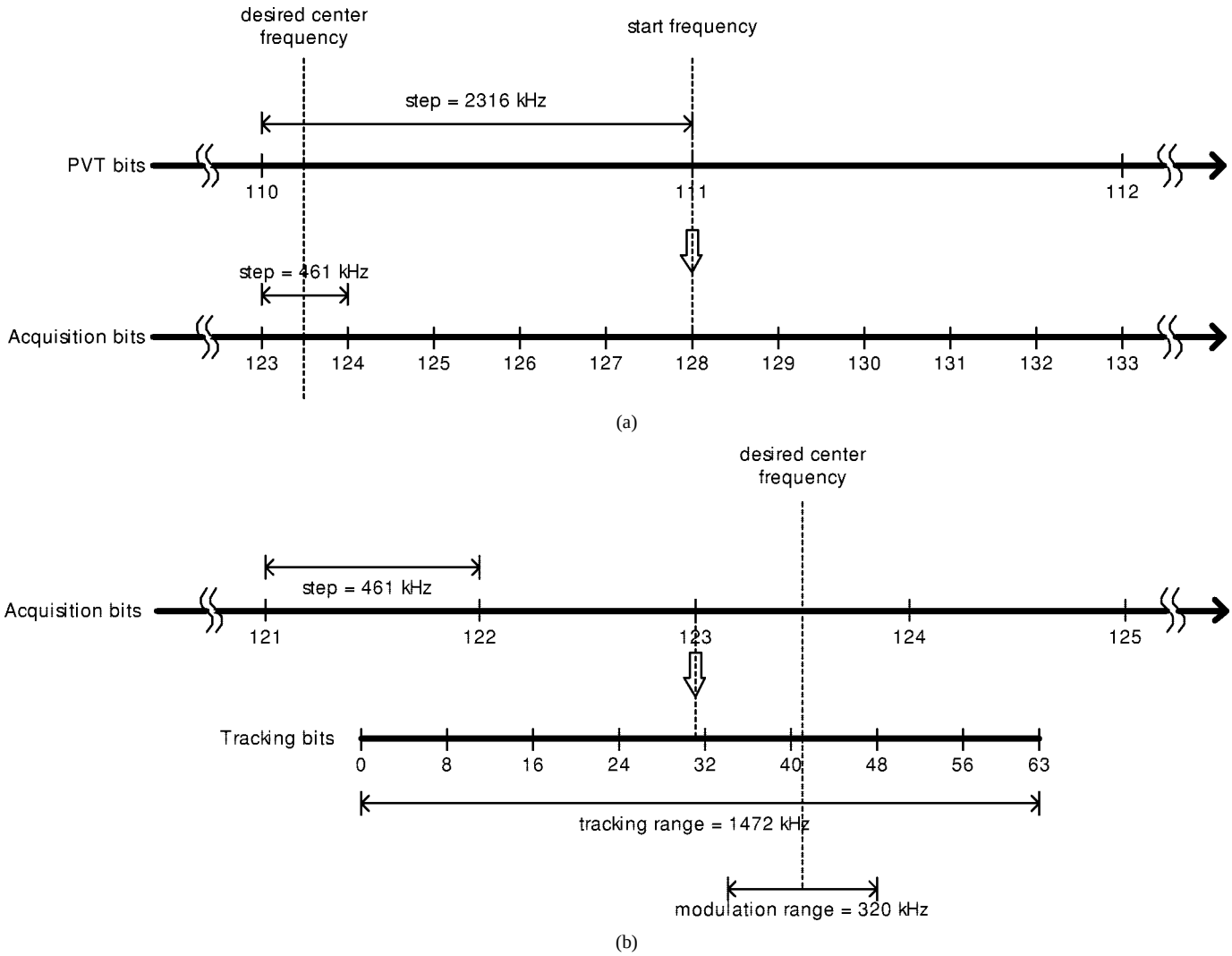

Fig. 9. Frequency transversal example for the implemented DCO. (a) PVT to acquisition. (b) Acquisition to tracking. PVT is calibrated to the middle of the BLUETOOTH band with code 111.

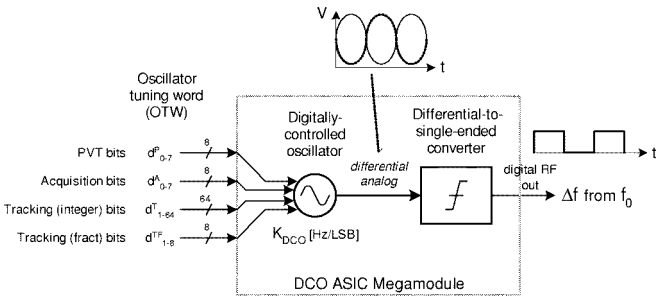

Fig. 10. DCO as an ASIC cell with digital I/Os.

that transforms the analog oscillator waveform into the zero-crossing digital waveform with a high degree of common-mode rejection.

The presented DCO allows for its loop control circuitry to be implemented in a fully digital manner. It should be emphasized that the DCO itself provides little restriction in the choice of a digitally intensive or an all-digital PLL-based frequency synthesizer architecture that could be employed. A classical PLL loop classification of type, order, and s-domain closed-loop transfer function could still be used for comparative purposes. In this study, a type-I first-order all-digital PLL structure operating in a synchronous phase domain (based on [13]) with the following closed-loop transfer function was utilized in order to close loop around the DCO:

$$H_{cl}(s) = \frac{N}{1 + \dfrac{s}{\alpha \cdot f_R}} \tag{38}$$

where N is the frequency division ratio, f_R is the reference frequency, and α is an attenuation factor of the proportional loop gain.

The 2.4-GHz DCO and its peripheral digital circuitry have been fabricated in a digital 0.13-μm CMOS process. Fig. 11 shows a die micrograph of the RF frequency synthesizer area. It is located in the lower left-hand-side corner and occupies 0.54 mm^2. The *LC*-tank inductor occupies a 270 μm $\times$ 270 μm square and is clearly discernible as the biggest single component on the entire chip. This photograph dramatically illustrates the high cost (in terms of digital gates) of conventional RF components in high-density modern CMOS processes (this process

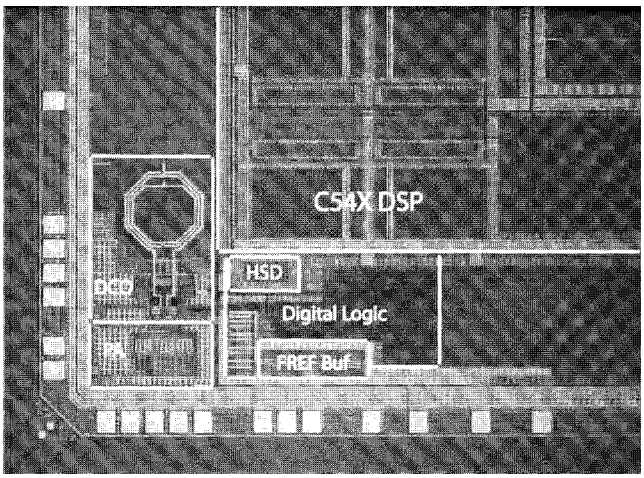

Fig. 11. Chip micrograph of the RF area (only lower left-hand-side corner of the chip is shown).

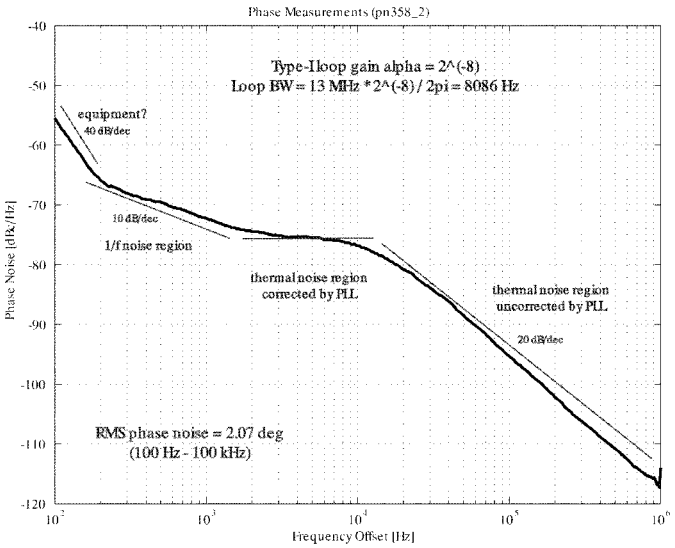

Fig. 12. Measured synthesizer phase noise with the presented DCO: wide loop bandwidth of 8 kHz.

features 150k gates/mm^2). Consequently, the number of classical RF components shall be minimized with proper architectural and circuit design choices. The synthesized RF output is buffered to the external pins through a class-E power amplifier (PA), which was chosen due to its digital-friendly characteristics. It is realized as an NMOS switch followed by a 50-Ω matching network. High-speed digital (HSD) logic running at 600 MHz (divided-by-four DCO clock) performs the $\Sigma\Delta$ dithering of the DCO varactors. The companion TMS320C54X DSP (used in cellular phones) digital baseband occupies 6 mm^2. This area comparison clearly illustrates the benefits of digital implementation of RF synthesizers.

IX. Measured Results

Measured phase noise of an all-digital frequency synthesizer with the presented DCO is shown in Fig. 12. The PLL loop forms a type-I first-order structure (single pole at dc due to the DCO oscillator frequency-to-phase conversion) with the 3-dB loop bandwidth of 8 kHz. The phase noise is -112 dBc/Hz at

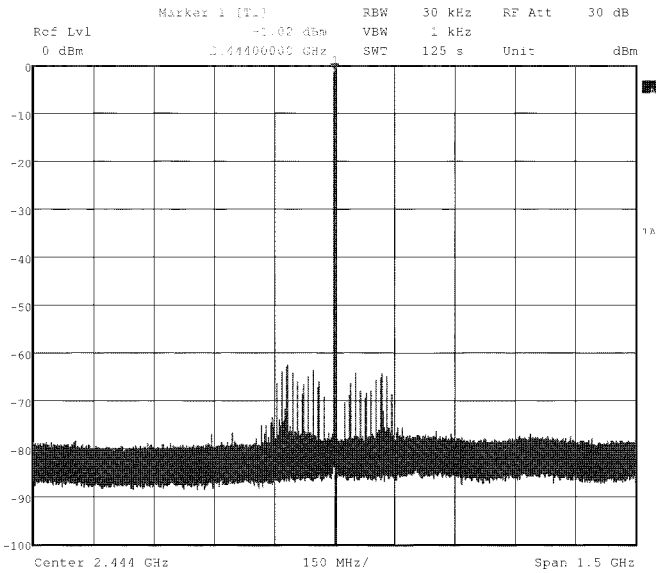

Fig. 13. Spurious tones generated by a synthesizer with the presented DCO using $\Sigma\Delta$ varactor randomization are invisible at 600-MHz offset while the close-in spurs are due to the suboptimal layout of power and ground lines.

500-kHz offset and is actually constrained by operating in the current limited region. Fig. 13 reveals the spurious tones emitted during the locked operation in the wide span of 1.5 GHz when the DSP is turned on. The close-in spurs lie below -62 dBc and are due to suboptimal layout of power and ground lines causing excessive FREF coupling. The spur level could be even lower if the layout is improved. The far-out spurs are vanishingly small and well below the floor of -80 dBc. The carrier power level is at -1 dBm. The settling was measured to be less than 50 μs. The DCO core consumes 2.3 mA from a 1.5-V supply and has a very large tuning range of 500 MHz. The presented DCO easily meets the BLUETOOTH spec.

X. Conclusion

A novel DCO architecture for multigigahertz RF applications has been proposed and demonstrated in this paper. This enables to employ fully digital frequency synthesizers in the most advanced deep-submicrometer CMOS processes with almost no analog extensions. It allows cost-effective integration with the digital back-end onto a single silicon die. A 2.4-GHz DCO and its peripheral circuitry that performs frequency synthesis have been fabricated in a digital 0.13-μm CMOS process and integrated with a digital signal processor (DSP). It demonstrates feasibility of the DCO in a digital synthesizer architecture for RF multigigahertz applications.

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